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The Implementation and Analysis of an All-digital Phase-locked Loop

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Abstract

An all-digital phase-locked loop (ADPLL) circuit is presented. The feature of the ADPLL is that its resolution in the phase detector and digitally controlled oscillator (DCO) exactly matches the gate-delay time. With the advances in eep-submicron technologies, the demand for high performance and short time-to-market integrated circuits has dramatically grown recently. The utilization of automated synthesis approach benefits from the standard cell-based design flow and hence implements a user-specified ADPLL within a short time. This paper presents a scheme to overcome the limitations of standard cells and to build up high resolution delay cell and high sensitivity phase and frequency detector (PFD). Since both the design time and design complexity of the ADPLL is greatly reduced, the proposed scheme is very suitable for System-On-Chip (SOC) applications.

Key words：All-digital phase-locked loop (ADPLL); Digitally Controlled oscillator (DCO); Phase and frequency detector (PFD)