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A Superscalar Micro-architecture Supporting Aggressive Instruction Scheduling

Chang, Meng-chou; Lai, Feipei

Abstract

A new micro-architecture, called IAS-S, has been found to support boosting efficiently. The new system employs a semantic register and a boosting boundary register to eliminate the dependencies caused by conditional branches. In IAS-S, there is no dedicated shadow register file. Multilevel boosting is supported without multiple copies of register files. Using a semantic register makes it possible to regard any general-purpose register in IAS-S as a sequential register or as a shadow register. Thus, idle registers can be used to help reduce spill code or to relieve storage conflicts. This is a distinct advantage over the dedicated shadow register file scheme, in which idle shadow registers cannot be used for such purposes. Furthermore, the IAS-S micro-architecture employs multi-way jump in conjunction with boosting to reduce the time delays due to frequent control transfers.

Key words：Superscalar processor;Instruction scheduling;Boosting;
Shadow register file