Combining the Folding and Testing for Programmable Logic Arrays

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Abstract

Different from the previous techniques which treated the folding and testing for PLAs as separate problems, this paper presents a new approach to combine the bipartite folding and testing for PLA's in the same procedure. Fewer silicon area than other existing comparable techniques is required to make the PLA testable. Experimental results show that this technique can reduce chip area, test length, test storage and time complexity.