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汽車 42V 電力電子高壓組件開發與其高可靠度技術之建立
HV Device Development and Its High Reliability Establishment in a Vehile 42V Power Electonic IC

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中文摘要

我們觀察到車用 IC 使用成本逐年在增高，因此未來車用 IC 在車輛產業將扮演著重要角色。電子應用在汽車上相當廣泛，其中以車用 MCU 市場最高，其次為類比 IC。目前車上所使用 12V 電源已經超過了 50 年的歷史，過去由於汽車上需用電的電子設備較少，12V 電源勉強還能滿足車上需求。但隨著相關電子設備導入車內，起動機的功率也逐年提高，12V 電源已無法滿足車體的需要，因而下一個電源世代中，受到矚目的是 42V 電源系統。歐洲汽車廠已開發出 42V 車用電源系統的相關標準，Benz 與 BMW 也都計畫將 42V 電源推向汽車市場中，日本和美國的汽車廠也將跟進，車用電源系統的世代交替之趨，似乎難以抗拒。因此在本年度的計劃中，我們將以此未來 42V 車用電源系統高壓驅動 IC 為發展及技術開發目標。從功率效應來評估，42V 電源所產生功率將達到 12V 電源 1 倍之多，提供了汽車電子設備更大的發展空間。在車用系統特性需求與應用領域上，IC 模組主要的關鍵技術包括了半導體功率元件技術，其中半導體功率元件扮演相當重要一環。Power MOS 功率電晶體一般被使用在輸出端驅動器上，此外此元件也被利用當做高壓 ESD 保護元件，但高壓功率半導體元件抗 ESD 的能力經常性地比一般低電壓製程之積體電路更為脆弱。然而，為了要有效分析 ESD 的特性，了解其寄生 BJT 的元件結構將會有相當大的幫助。由於車用電子之 Power MOS 功率元件在應用上，本身周遭環境及外來突波均有可能產生異常高的電壓。因此功率元件也必須考量抗高靜電放電(ESD)破壞及突然外來過壓破壞(EOS)之能力。以往高壓功率元件有著很差的 ESD 防護能力，因此本計劃擬提升 Power MOS 功率元件之 ESD/EOS 防護能力，使其之具有較佳的可靠性。靜電放電的問題日益嚴重，傳統靜電防護元件的設計大多利用嘗試錯誤法實際測試或用 SPICE 模擬等效電路，以獲得可能適合的保護元件。本研究先利用 Tsuprem-4 及 MEDICI 等 EDA 模擬

軟體設計出 Power MOS 電性參數值，而且由 TLP 量測找出 Design Widow 中適切的 ESD 保護元件參數，再利用佈局參數分析比較其結果，使保護元件的電性表現符合 Design Window 範圍來達到 Power MOS 的 ESD 保護最佳化的目的。在汽車電子功率元件技術中，高效能的 ESD 保護結構應該具有一個高於 42V 的保持電壓(可由 TLP 測試可量得)。這能確保一個良好的 ESD 保護效能在高電壓峰值時不會有發生另一個可靠性 Latch-up 的危險。本計劃中將提出最佳化方法去達到這樣的目的，對於功率結構的分析，針對 ESD 應力下我們使用 TLP 測量工具，HBM 測試， EMMI 測量和 2D-元件模擬來研究 42V/數安培-Power MOS 功率電晶體詳細的物理結構。最後希望此功率技術產品的 ESD 性能可通過 > 6KV、保持電壓> 60V, 最小驅動電流 1 安培。根據此研究，我們將提出一個有關 ESD-Power MOS 簡潔模型，這個模型成功的描述出 Power MOS 的高電流、高電壓特性。

關鍵字：車用高壓組件; 靜電放電; 過壓破壞; 閂鎖效應; 人體模型; 快速傳輸線脈衝

Abstract

The used cost of vehicle IC increases year by year, so it will be an important role that automobile-used IC acted in the vehicle industry in the future. It is very quite extensive that the electronics is applied to the automobile, among this it is the highest with automobile-used MCUs market, secondly it is the analog ICs. Almost more than 50 years history of 12V power used in the car until present, because there is less electronic equipments needing to be used the electricity on the automobile, 12V power still can meet the demand on the car reluctantly. But as the relevant electronic equipments are built into the car and the power of the starter imcreased year by year, 12V power has been already unable to meet demands of car body, but in the next power generation, it is 42V power system that is attracted attention. The European automobile factory will already develope the relevant standard of 42V automobile-used power system, such as Benz and BMW all plan to push 42V power to the automobile market, and then Japan and automobile factory of U.S.A. will follow up, Therefore, we will aim these goals in this research year. Power MOS transistors of vehicle technologies are commonly used as output drivers such as in high-performance applications. Futhermore, this device

will be also employed as the ESD protection element in the high voltage O/P pins. However, medium sized drivers often show a striking ESD vulnerability. This is attributed to inhomogeneous triggering of the parasitic BJT. Nevertheless, in many conditions the ESD immunity level of power semiconductor components may be lower than the low-voltage CMOS IC. Therefore, it is useful to analyze possible options to optimize the ESD behaviour. The modern power integrated circuits in vehicle electronics can endure with somewhat high voltage. Nevertheless, it is known that the electrostatic discharge (ESD)/ electric over stress (EOS) may be the most insidious failure mechanism of power ICs. However, the ESD/EOS robustness is very poor in the input/output ports of a power device. Therefore, in this work, we will present the design of efficient ESD/EOS protection of power device, also they will be good for the latch-up immunity. In this work, the EDA simulators such as TSUPREM 4 and MEDICI are used to simulate and improve the electrical property of Power MOS devices and to design an optimized ESD protection circuit. By these procedures, the varied layout parameters of ESD protection device should be met the design window and to reach the optimum of ESD protection. In the automotive applications, power component technology, highly efficient ESD protection structures with a holding voltage >42V will be realized in a smart power technology. They guarantee an excellent ESD protection at high voltage pins without the danger of transient latch-up. Some methods are to achieve this goal by suitable design. For the analysis of the structures, beside HBM testing, the recently developed TLP will be employed. It it hopes that this Power MOS to be technological ESD performances of product can pass HBM > 6KV, Vh > 60V, and current driving capability with one amperes minimumly. Finally, an ESD-Power MOS compact model will be developed, and which will successfully describe the Power MOS high current behaviour.

Key words：Vehicle HV Module; ESD; EOS; Latch-up; HBM; TLP