國科會計畫
計畫編號: NSC100-2221-E239-003
研究期間: 10008-10107

高可靠性低驟回之車用高壓 nLDMOS 元件研究
A Study of High Reliability &Amp; Weak Snapback in an Nldmos Device for the Vehicle Hv Application

陳勝利; 陳宏偉; 陳勛祥

中文摘要

下一個車用電源世代中，現受到相當矚目的是 42V 電源系統，歐洲汽車廠已開發出 42V 車用電源系統的相關標準，日本和美國的汽車廠也將跟進，車用電源系統的交替趨勢主流，似乎難以抗拒。但除了電源功率，穩定性、安全可靠度等，各項因素都是未來決定性的關鍵。因此在本年度的計劃中，我們將接續之前的計劃經驗，延續此未來 42V 車用電源系統高壓驅動 LDMOS 之高 Latch-up 免疫力/靜電防護能力研究為發展開發目標。未來車用系統特性需求與應用領域上，主要的關鍵技術包括了高壓功率元件技術，其中操作電壓超過 18V，因此 LDMOS 半導體功率元件扮演相當重要角色。LDMOS 功率電晶體一般被使用在輸出端驅動器上，但高壓功率半導體元件抗 Latch-up/ESD 的能力經常比一般低電壓製程之積體電路更為脆弱。由於車用電子之功率元件在應用上，周遭環境有可能產生異常高的突波電壓。因此 nLDMOS 功率元件必須擁有高 Latch-up 免疫力/靜電防護能力，使其之具有較佳的可靠性。在汽車電子功率元件技術中，高效能的功率元件結構應該具有一個高於 42V 的保持電壓(Vh)及較低的觸發導通電壓值(Vt1)，因此最好此結構最好擁有弱驟回性(weak-snapback)特性，這能才能確保一個良好的 ESD 保護效能在高電壓峰值時不會有發生另一個可靠性 Latch-up 的危險。傳統可靠性的設計大多利用嘗試錯誤法實際測試或進階點用 SPICE 模擬等效電路，以獲得可能適合的元件。本研究將先利用 Tsuprem-4 及 MEDICI 等 EDA 模擬軟體設計出 nLDMOS 結構參數值，並以田口法去達到結構最佳化(弱驟回性(weak-snapback)特性)目的。對於此實際 42V nLDMOSFET 的 Latch-up 免疫力/靜電防護力分析，我們將使用快速脈衝測量儀、HBM 測試來驗證之。

關鍵字：車用電源; 橫向擴散金氧半電晶體; Latch-up 免疫力; 靜電防護; 保持電壓(Vh); 觸發導通電壓值(Vt1); 弱驟回性; 田口法; 快速脈衝量測儀; 人體靜電模型

Abstract

In the next power generation, the 42V power system that is more attracted attention in the vehicle industry. The European automobile factory will ready develope the relevant standard of 42V automobile-used power system, and then Japan and automobile factory of U.S.A. will follow up, too. But except the power, stability , safe reliability ,etc., every one factor is decisive key in the future. So in the plan of this current year, we will continue the past experience of the previous year, extending this high systematicly 42V automobile-used power and focusing on the high latch-up immunity/ESD protective capacities of a new weak-snapback LDMOS. Power MOS devices of vehicle technologies are commonly used as output drivers such as in high-performance applications. The operation voltage will above 18V, so the LDMOSFET will be act as a good candidate. Futhermore, this device will be also employed as a protection element in the high voltage O/P pins. Nevertheless, in many conditions the Latch-up/ESD immunity level of LDMOSFETs may be lower than the low-voltage CMOS IC. In the vehicle applications, highly efficient power device structures should be with a holding voltage, Vh >42V, and a lower trigger voltage(Vt1) in a smart power technology. A no-snapback behavior, they guarantee an excellent ESD protection at high voltage pins without the danger of transient latch-up. In this study, the EDA simulators such as TSUPREM 4 and MEDICI are used to simulate and improve the electrical property of nLDMOS devices, in the meanwhile the Taguchi method will be used to design the optimized structures with weak-snapback characteristics. For the analysis of the structures, beside HBM ESD testing, the recently developed fast pulse system for LU testing will be employed.