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Combined Use of Rising and Falling Edge Triggered Clocks for Peak Current Reduction in IP-Based SoC/NoC Designs

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Abstract

In a typical SoC (System-on-Chip) design, a huge peak current often occurs near the time of an active clock edge because of aggregate switching of a large number of transistors. The number of aggregate switching transistors can be lessened if the SoC design can use a clock scheme of mixed rising and falling triggering edges rather than one of pure rising (falling) triggering edges. In this paper, we propose a clock-triggering-edge assignment technique and algorithms that can assign either a rising triggering edge or a falling triggering edge to each clock of each IP core of a given IP-based SoC/NoC (Network-on-Chip) design. The goal of the algorithms is to reduce the peak current of the design. Our proposed technique has been implemented as a software system. The system can use an LP technique to find an optimal or suboptimal solution within several seconds. The system also can use an ILP technique to find an optimal solution, but the ILP technique is not suitable to be used to solve a complex design. Experimental results show that our algorithms can reduce peak currents up to 56.3%.

Key words：Clock scheme; Globally asynchronous locally synchronous; IR drop; Network-on-Chip