5th Taipei International Digital Earth Symposium (TIDES 2007)
Pages 27-36, May 2007

A Step-by-Step RS Decoder for High-Speed Digital Transmission Systems
適用於高速數位傳輸系統之步階式里德-所羅門解碼器

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Abstract

Reed-Solomon (RS) code is one of the most frequently employed forward-error-correcting (FEC) codes in digital transmission and storage systems. A well-known decoding method, the step-by-step algorithm, can decode the RS code in a symbol-by-symbol manner with low latency delay. This method can directly determine whether the received code symbol is erroneous or not and immediately find the corresponding error value without requiring of finding the error location polynomial. Based on a modified step-by-step RS decoding algorithm, a high-speed pipelined (32,24,4) RS decoder is implemented. According to the high-speed step-by-step RS decoding procedure, we use VDHL hardware design language to design the RS decoder. To speed up the operation, we adopt the pipeline structure and choose operators with cellular-array multiplier, systolic multiplier and systolic power-sum circuit. The decoder only requires the delay time of three gates for decoding each coded symbol. Therefore, this pipeline RS decoder can provide a high decoding speed of Gbits/sec order and can apply to the high-speed digital transmission systems. Finally, it is implemented by LYRTECH's TMS320C6713/VIRTEX-II Based SignalWAVe board. We used Simulink and Xilinx tools to complete the hardware implementation and software/hardware co-simulation of the high-speed step-by-step (32, 24, 4) RS decoder with LYRTECH's SignalWAVe board.

Key words：Reed-Solomon code; Step-by-step; Decoder; FPGA; High-speed