N-channel Fluorinated Copper Phthalocyanine Thin-Film Transistors Utilizing Oxygen-Plasma-Treatment ITO Source and Drain Electrodes

Wang, Yu-Wu; Yen, Chen-Hsiang; Chou, Wei-Yang; Cheng, Horng-Long; Liu, Shyh-Jiun

Abstract

In this study, device characterization and carrier transport properties of n-type fluorinated copper phthalocyanine (F16CuPc) organic thin-film transistors (OTFTs) were investigated using bottom gate device configuration with oxygen-plasma-treatment indium-tin-oxide (ITO) bottom source and drain (S/D) contact. We fabricated F16CuPc-based OTFTs having comb-shaped channels with a series of channel lengths of $5\square 100 \mu m$ at a fixed channel width. The electrical characteristics of OTFTs were measured by a Keithley 4200-SCS semiconductor parameter analyzer in a dark glove box in a nitrogen atmosphere to avoid the influence of measuring environments. The device characteristics were analyzed using the charge-sheet metal-oxide-semiconductor field-effect transistor model equation. We found that both the linear and saturation field-effect mobilities and threshold voltages of F16CuPc-based OTFTs increased with increasing channel length. The linear and saturated field-effect mobilities were gate-bias dependent in all devices with different channel dimensions. Moreover, the contact resistance between ITO S/D electrodes and F16CuPc and channel resistance of F16CuPc were investigated using the gated-transfer length method. The results of our experiments suggest that the contact resistance between ITO electrodes and F16CuPc plays an important role in current-voltage characteristics. Additionally, abnormal increases in saturated field-effect mobility at channel lengths below 10 µm were observed in our experimental devices and were attributed to short channel effects. Such non-ideal effects of the present F16CuPc-based OTFT devices were investigated in detail. In summary, we found that the oxygen-plasma-treatment ITO bottom contact S/D electrode-based F16CuPc OTFT devices were very durable and suitable to make large area transistor arrays with complicated integrated circuits by photolithography techniques.