國科會計畫
計畫編號: NSC97-2221-E018-027
研究期間: 9708-9807

奈米製程中兼具電流易測性與低峰快醒的電源閘控功耗管理系統之研究
High-Current-Testability Low-Spike Wakeup-Accelerated Supply-Gating Power Management

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中文摘要

本計畫為一年 A 類計畫，執行期間為民國九十七年八月一日至民國九十八年七月卅一日，研究主題為「奈米製程中兼具電流易測性與低峰快醒的電源閘控功耗管理系統之研究」，主要目的在於設計具有睡眠電流易測性之降低尖峰、快速甦醒之微粒電源閘控邏輯元件，以提供奈米製程單晶片功耗管理系統一個低功、高速與高品質的元件庫與參考流程。我們發現：同時達到電流易測性、低尖峰電流與快速甦醒的關鍵在於雙邊微粒電源閘控元件之自我調適資料保持性，在腹案中，我們已將據此廣泛分類分析與比較，發展各式低功高速與高品質之邏輯元件庫；接著我們將發展適用於奈米製程之內建電流感測器，並建立最佳化叢聚架構，以小型處理器系統與各式小型測試電路進行佈局實現；進而設計流程自動化與雛型晶片量測分析，並據以改進所發展出來的結構與工具。本計畫研究成果可能成為未來奈米製程參考設計流程之一，提供生醫航太等低功高速與高品質的快速合成設計，更可增進台灣可攜性消費電子業在國際間的競爭力。

關鍵字：超閉路開關; 通閉路電流比; 低功高速; 多門檻電壓金氧半電晶體; 電源閘控; 雙邊微粒電源閘控; 尖峰電流; 加速甦醒; 靜態電流測試法; 睡眠電流測試法; 電流易測性設計; 睡眠模式; 次門檻漏電流; 資料維持性; 參考設計流程; 叢聚式電源閘控

Abstract

This proposal is for a 1-year class-A research project entitled “High-Current-Testability Low-Spike Wakeup-Accelerated Supply-Gating Power Management System in Nanotechnology.” The major objectives are to develop a novel current test scheme in sleep mode and a set of fine-grained power-gating logic structures simultaneously for high current testability, low spike and accelerated wakeup time for the reference design flow of the power management system in nanotechnology. The key point of the simultaneous current testability, low spike and accelerated wakeup is the self-adaptive data retention of the bilateral fine-grained power-gating logics. Based on this point, we have generally analyzed the potential structures and developed a set of low-power high-speed high-testability logic cell library in advance. In this project, we will aim at developing the built-in current sensor for nanotechnology. Finally, the developed library design and flow will be automated and the prototyping chips will be measured and analyzed for improving our theory, structures and design flow. The developed results can potentially become one of the reference design flows for future nanotechnology. The related technologies cannot only potentially provide a low-power high-speed and high-testability cell-base syntheses for biomedical and aerospace electronics but also highly promote the international competitiveness of the custom electronic industry in Taiwan.

Key words：Super-cutoff; On/off current ratio; Low-power; High-speed; MTCMOS; Zigzag; Power-gating; Supply-gating; Bilateral fine-grained power-gating; Powermanagement; Spike reduction; Wakeup acceleration; IDDQ test; Design forcurrent testability; IDDS test; Sleep mode; Subthreshold leakages; Data retention; Keeper; Reference design flow; Clustering