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低功耗低成本高可靠度內容可定址記憶體之研究
Low-Power, Low-Cost and Dependable Design of Content-Addressable Memory

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中文摘要

在需求為發明之母的動力下，近一、二十年來，電腦、通訊及消費性電子 3C 技術急遽蓬勃發展。其中，內容可定址記憶體乃電腦結構、通訊網路、數位訊號處理、資料庫搜尋、乃至於記憶體修復等各種快速平行查表與轉接等功能所共同需求之子系統電路技術。其中，二值內容可定址記憶體常用在快取、色譜器及內建自我修復中；而三值內容可定址記憶體則常用在路由器、防火牆與內容可定址網路上。本計畫主要內容有四：其一乃針對內容可定址記憶體提出以預先編碼為基礎之降低成本與功耗的技術；其二提出一種大小比較式的內容可定址記憶體，可以在結構與協定上降低成本與功耗；其三提出此種大小比較式的內容可定址記憶體在色譜器與測試領域的應用；最後為研究上述各內容可定址記憶體的錯誤模型與測試方法。包含腹案已產出之兩篇 SCI 論文外，本計畫預計能再衍生兩篇以上的 SCI 論文；更希望能將技術轉移工業，造福人群。

關鍵字：內容可定址記憶體; 大小比較式內容可定址記憶體; 記憶體修復

Abstract

Recently the consumer, computer and communication electronics industry have risen quickly. In the 3C electronics, the content-addressable memory has become the most important circuitry for computer architecture, communication network, digital signal process, database sorting and searching and many look-up interfaces. Generally the binary content-addressable memory is useful in caching, histogrammer and built-in self-repair while the ternary in IP routing, firewall and content-addressable network. This project is mainly i) to propose a multi-valued equal-weight code for reducing the cost and power dissipation of content-addressable memory, ii) to develop a novel magnitude-comparator-based content-addressable memory that can highly reduce the cost and power by shrinking inference entries under proper protocols, iii) to extend the applications of the above techniques in histogramming and testing, and iv) to study the fault model and testing methods for the invention. Except two published SCI journal papers, more than two SCI papers are planned to be created from this project. Furthermore we hope the developed techniques and associated training can improve the life of our people by transferring to the industry.

Key words：CAM; Content-Addressable Memory; Magnitude-Comparator-Based Content Addressable Memory; Memory Repair