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混合記憶體立方體內建自我修復之研究
Study on Built-In Self-Repair for Hybrid Memory Cubes

黃宗柱

中文摘要

隨著消費者的需求與多元電子科技的快速整合，智慧電子已成為全球關注的焦點，也是國家未來十年的重點計畫；而由於適應規格日益嚴格、要求速度與容量日漸提昇，積體電路在高速、低功與縮小化的需求下，三維(3D)晶片自然成為發展的主軸。其中，記憶體非僅是 3C 電子、車用電子的主體之一，也是多數生醫電子不可或缺的單元，尤其是其需求容量常隨著智慧與資料等級激增。最近，混合式記憶體立方體(Hybrid Memory Cube, HMC)，其省電效率與傳輸速度將使其成為記憶體設計的新模式。本計畫之目的在於有系統地探討與評估提昇混合式記憶體立方體等效良率之技術。本計畫之目的有二：其一在於有系統地探討與評估提昇記憶體等效良率之技術；其二在於提出 TSV 自我修復的方法。本研究團隊於近年研究計畫已發展出低成本高可靠的修復與容錯技術，最近研究的腹案，對 TSV 的冗餘分析也有突破的發展，希望提出此計畫，對國家工業有所貢獻。包含腹案已產出之一篇 SCI 論文外，本計畫預計能再衍生兩篇以上的 SCI 論文；更希望對於本土智慧電子產品、可攜式消費性電子產品與高速、高密度晶片的量測技術有即時的幫助；尤其如獲相關產業的合作與技轉，將對國內記憶體產業有提昇產能的直接幫助。

關鍵字：三維積體電路; 記憶體修復; 位址映射結構; 大小比較式內容可定址記憶體; 位址集中器; 超方體; 良率; 修復率; 內建冗餘分析; 容錯; 混合式記憶體立方體; 矽穿孔; 矽載板; 通道集中器

Abstract

Recently the intelligent electronics has become one major focus in the world and even the key national project, where the memory will be not only the key core in 3C electronics, automotive electronics and the cloud center, but also an indispensable unit in most bioelectronics. Especially the memory volume is usually increasing according to the intelligent level such that the hybrid memory cube, HMC, has become the novel and efficient solution. Owing to the stricter specification, required speed and huge capacity, and even the high security and reliability for the automotive electronics and bioelectronics, the product yield and reliability of the embedded memory have become a crucial challenge in the roadmap of the developing for intelligent electronics. The purpose of this project is to study and develop the technology for yield enhancement of the HMC. The major contents consist of two major subprojects. The first subproject will continue and extend the research of the project in 2011. In the first subproject, a novel memory address remapping architecture is developed for Gray-coded ordered memory. The redundancy analysis and repair algorithms will be developed. Then the issues including the built-in self-test for the built-in design for memory repair and the time penalty over access time will be studied and solved. In the second subproject, a remapping architecture similar to the above ARU is also developed for the TSV interconnections. Then we will involve in redundancy analyses of a variety of TSV and other elements in the 3D HMCs. Except one published SCI journal papers, more than two SCI papers are planned to be created from this project. Furthermore we hope the developed techniques and associated training can improve the life of our people by transferring to the industry.

Key words：3D IC;Memory Repair; Address Remapping Architecture; Comparator-based CAM; Address Concentrator; Hypercube; Yield; Repair Rate; Built-In Redundancy Analysis; Fault-Tolerant; Hybrid Memory Cube; HMC; TSV; Interposer; Chanel Concentrator; Parallel Sorter