國立成功大學電機工程學系博士

CMOS 邏輯電路之低功率測試
Low Power Testing for CMOS Logic Testing

黃宗柱

中文摘要

在系統單晶片(SOC)的時代，電晶體密度的提高與操作速度的增加使得功率消耗成為測試時一項關鍵性的問題。本論文主要針對此一問題，提出四項技術以減少 CMOS 邏輯電路在測試時的功率消耗。茲摘要此四項技術如下：首先，我們提出輸入端控制技術(Input control technique)，此技術採用一個類似 D 演算法的方法來產生一個控制向量，在掃描電路時輸入在主輸入端，以便儘量阻斷掃描時的跳動，降低組合邏輯電路的平均功率消耗。此技術可以與既有之向量排序法與栓鎖排序法並用。實驗結果顯示，既有之向量與栓鎖排序法可以減少 22.37%的功率消耗；當在栓鎖與向量排序法之後採用輸入端控制技術時，將可降低 34.23%的平均功率。

其次，在降低多鏈掃描電路的尖峰功率方面，我們提出一項錯開掃描技術(Interleaving scan technique)。此技術主要藉由在各掃描鏈間加入一或兩個 D 型正反器作為延遲緩衝器以錯開各掃描鏈之尖峰功率發生的時間，使整體尖峰功率得以有效降低。由實驗得知，當掃描元件的資料輸出會受到掃描輸出影響時，最高可降低 51%的尖峰功率；當掃描元件的資料輸出不會受到掃描輸出影響時，最高可降低 76%的尖峰功率。

第三種技術提出一種符記掃描架構(Token scan architecture)，此架構結合多相時序、符記環及時脈閘控等三項技術，以降低資料跳動、減輕繞線及相間時差(Skew) 的問題、並消除廣播型態之功率消耗。由實驗得知，當掃描鏈很長時，平均功率將可降低超過 95%。

另外，我們也對內建自我測試提出一種低功率消耗的多相混成線性回授移位暫存器(Multiphase hybrid LFSR)。由於前人之多相線性回授移位暫存器需要比較複雜的多相時脈產生器及控制邏輯電路與傳輸閘式的多工器，使得功率降低率有限。我們設計了一個由栓鎖式強生計數器所實現之多相時脈產生器，並使用靜態邏輯閘所組合之解多工器，提出一個單相與多相混成之線性回授移位暫存器。由評估分析中得知，當正反器個數大於 27 時，我們的架構比前人的方法降低 40%的功率消耗；若是與傳統單相之設計比較，將可降低 70%的功率消耗。

整體而言，輸入端控制技術主要目的在降低測試時的平均功率消耗；相對的，錯開掃描技術可以有效降低尖峰功率；符記掃描架構與多相混成線性

回授移位暫存器則可以有效降低平均功率而其尖峰功率降低率也很可觀。最後我們將此四種技術的功率降低率與其應用性列表討論，並經由這些分析提出未來改進與研究的方向。

觀鍵字：低功率測試; 超大型積體電路測試; 易測試性設計; 功率消耗; 掃描式電路; 內建自我測試; 系統單晶片測試; 測試功率

Abstract

The increasing transistor density and operating speed in the system-on-a-chip (SOC) era make the power dissipation during test a critical issue. This dissertation proposes four techniques to reduce the power dissipation in test application time for CMOS logic circuits.

First, we propose an input control technique that employs a D-algorithm-like approach to generate a control pattern which, when applied at the primary inputs during scan operations, can minimize the switching activity of full-scan circuits. This technique can be utilized together with the existing vector ordering or latch ordering techniques. Experimental results show while the vector ordering and the latch ordering techniques can achieve 22.37% of average power reduction, 34.23% average improvement can be achieved if the input control technique is employed after the latch ordering and vector ordering techniques.

Second, an interleaving technique is proposed to reduce the peak power of multiple scan chain based circuits during testing. A test architecture is presented which can significantly reduce the peak power by adding delay buffers among the scan chains. This method can be efficiently integrated with a recently proposed broadcast multiple scan architecture due to the sharing of scan patterns. The effects of the interleaving scan technique applied to the conventional multiple scan and the broadcast multiple scan with 10 scan chains are investigated. Up to 51\% peak power reduction can be achieved when the data output of a scan cell is affected by the scan path during scan. When the data output is disabled during scan, up to 76% of peak-power reduction is observed.

Third, a novel token scan architecture is developed which employs the concepts of multiphase clocking, token ring and clockgating to minimize the data transitions, to alleviate the routing and skew problems, and to eliminate the broadcasting dissipation on the clock tree and scan-in data tree during scan operations. This token scan architecture can efficiently reduce the data transitions in the scan circuits as well as the switching activity in both the clock and the scan-in data trees. From experiments, more than 95% of power reduction can be achieved for most circuits with long scan chains.

Fourth, we observe that previously multiphase LFSR schemes have been proposed to reduce the data transitions during test and signal process. However, due to the more complex clock generator, the broadcasting input and the multiplexing output, the power reduction is actually much limited. We propose a new LFSR architecture to improve the power reduction via developing a novel low-power and cost-effective Johnson counter for the multiphase clock generator and employing static logic gates to implement the output multiplexer. To reduce the stages of the multiphase clock generator and the area of the multiplexer, a hybrid LFSR design combining both single and multiple phase clocks is developed. From our evaluation, our architecture has 40\% more power reduction than the previous n-phase LFSR architecture when n is greater than 27 and up to 70% power reduction compared to a conventional LFSR.

In summary, the input control technique is mainly for reducing the average power dissipation while the interleaving technique is for the peak power. Both the token scan architecture and the hybrid LFSR scheme can reduce average power as well as peak power. To conclude this dissertation, we tabulate the reduction efficiency of our techniques and analyze their applicability and suitability. Based on the analysis, some future work is suggested.

Key words：Low power test; VLSI test; Design for Testability; Power dissipation; Scan based circuits; Built-In Self-Test; SOC test; Test power